

03DET22F1043

CHONG KHENG CHEN

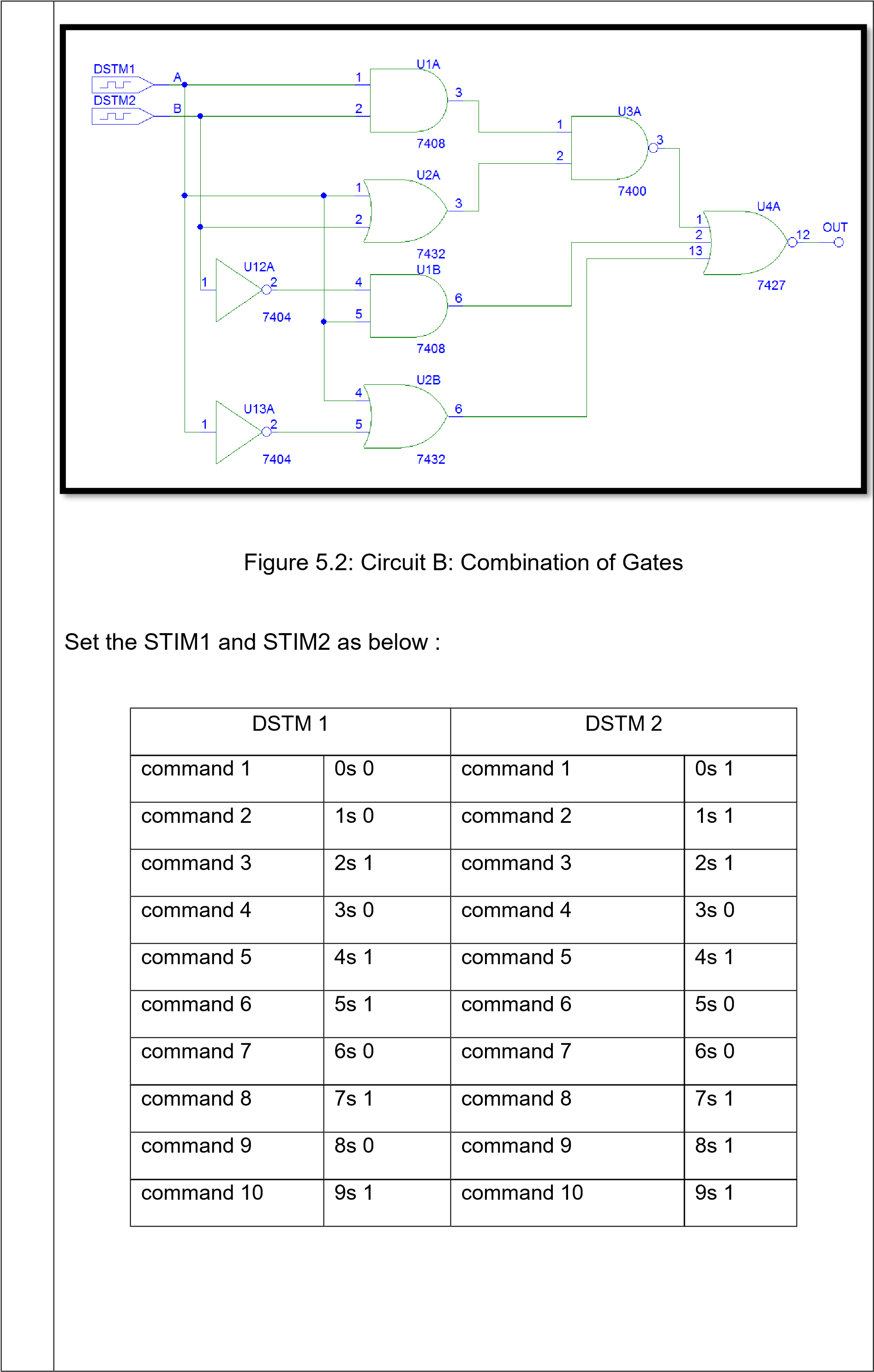
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| CLO1 (C3, PLO1) | COGNITIVE ASSESSMENT  (20 %) |  |
| CLO2 (P4, PLO5) | PSYCHOMOTOR ASSESMENT (80  %) |  |
|  | TOTAL MARKS  (100%) |  |

**\*Refer to Rubric**

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| **1** | **LEARNING OUTCOMES (LO):**    1. Apply the simulation results for the various types of simulation analysis based on the electronic circuit theory and operations |
| **2** | **OBJECTIVE :**     1. Apply the simulation result for digital simulation analysis using the Truth Table. 2. Construct the digital schematics circuit and simulate the circuits using a particular simulation packages. |
| **3** | **THEORY :**    A digital circuit simulation is an event-driven, time-domain simulation. You can define an arbitrary time step for your live digital simulation and increment the simulation time discretely, one step at a time, and manually change the state of the input(s) at each time step.  Through the experiment, students can learn the concept of digital circuit simulation, applications of logic level simulation for combinational and sequential logic circuits. Logic inputs can be represented as Digital Clocks and output can be obtained by performing Time Domain Analysis. The analysis produced is displayed as a timing diagram and later can be represented into a Truth Table. |
| **4** | **EQUIPMENT / TOOLS / SOFTWARE :**   1. PC workstation 2. Related software |

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| **5** | **PROCEDURE :**    Draw and simulate this logic circuit below:  i. Circuit A: (Figure 5.1) ii. Circuit B: Combination of Gates (Figure 5.2)    **PART A: DIGITAL CIRCUIT**  Construct the Truth Table for each circuit based on timing diagram obtained in Result section.    **PART B: DIGITAL CIRCUIT SIMULATION**  Sketch the timing diagram for each circuit in Result section.  Figure 5.1 Circuit A    Set the attributes for digclock parameter as below:   |  |  |  |  | | --- | --- | --- | --- | | DSTM1 | | DSTM2 | | | OFFTIME | 0.5us | OFFTIME | 0.1us | | ONTIME | 0.5us | ONTIME | 0.1us | | DELAY | 0 | DELAY | 0 | | STARTVAL | 0 | STARTVAL | 0 | | OPPVAL | 1 | OPPVAL | 1 | |

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|  | Click **Menu Bar**, select **Analysis**\**Setup**. Click check box **Transient** to enable it and set the specifications as shown below:    Print Step : 0.1us  Final Time : 2.0us  No Print Delay : 0  Step Ceilling : 0    Simulate the circuit and observe the output waveform. |



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| **6** | **RESULT :**  **PART A:**  Table 5.1: Truth Table for Circuit A:   |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | **Time** | **A** | **B** | **C** | **D** | **E** | **F** | | 0.1us | **1** | **0** | **0** | **1** | **1** | **0** | | 0.2us | **1** | **1** | **1** | **0** | **1** | **1** | | 0.3us | **1** | **0** | **0** | **1** | **1** | **1** | | 0.4us | **1** | **1** | **1** | **0** | **1** | **1** | | 0.5us | **0** | **0** | **0** | **1** | **1** | **0** | | 0.6us | **0** | **1** | **1** | **1** | **1** | **0** | | 0.7us | **0** | **0** | **1** | **1** | **0** | **1** | | 0.8us | **0** | **1** | **1** | **1** | **1** | **0** | | 0.9us | **0** | **0** | **1** | **1** | **0** | **1** | | 1.0us | **1** | **0** | **0** | **1** | **1** | **0** | | 1.1us | **1** | **0** | **0** | **1** | **1** | **0** | | 1.2us | 1 | **1** | **1** | **0** | **1** | **1** | | 1.3us | **1** | **0** | **0** | **1** | **1** | **0** | | 1.4us | **1** | **1** | **1** | **0** | **1** | **1** | | 1.5us | **0** | **0** | **0** | **1** | **1** | **0** | | 1.6us | **0** | **1** | **1** | **1** | **1** | **0** | | 1.7us | **0** | **0** | **1** | **1** | **0** | **1** | | 1.8us | **0** | **1** | **1** | **1** | **1** | **0** | | 1.9us | **0** | **0** | **1** | **1** | **0** | **1** | | 2.0us | **0** | **1** | **1** | **1** | **1** | **0** | |

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|  | Table 5.2: Truth Table for Circuit B: Combination of Gates   |  |  |  | | --- | --- | --- | | INPUTS | | OUTPUT | | A | B | OUT | | 0 | 1 | 1 | | 1 | 1 | 1 | | 0 | 0 | 1 | | 1 | 1 | 1 | | 1 | 0 | 1 | | 0 | 0 | 1 | | 1 | 1 | 1 | | 0 | 1 | 1 | | 1 | 1 | 1 |     **PART B:**   1. Timing diagram for Circuit A:          1. Timing diagram for Circuit B : Combination of Gates. |

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| **7** | **DISCUSSION :**  In DUSCUSSION, The Truth Table is used to compare input combinations and output values, while the digital schematics circuit ensures correct design and component connections. The simulation package provides features for functional, waveform, and timing analysis. By using these tools, it can be verified if the digital circuit functions as intended, and any design errors or discrepancies can be identified and corrected.by applying the simulation results for digital simulation analysis using the Truth Table and constructing the digital schematics circuit, we can verify if the digital circuit functions as intended. The simulation results can also help us identify any design errors or discrepancies and make necessary corrections. | | | | | | | |
| **8** | **CONCLUSION :**  IN CONCLUSION by applying the simulation results for digital simulation analysis using the Truth Table and constructing the digital schematics circuit, we can verify if the digital circuit functions as intended. The simulation results can also help us identify any design errors or discrepancies and make necessary corrections. | | | | | | | |
| **PRACTICAL WORK 4 : DIGITAL CIRCUIT SIMULATION** | | | | | | | | |  | A | |  | B |
|  | **MATRIX NUMBER** | | | | | **NAME** | | |  |
| **A** | **03DET22F1043** | | | | | **CHONG KHENG CHEN** | | |  |
| Course Learning  Outcomes(CLO)/  Learning Domain Cluster (CLS) | | | | Circuit | Skills /  Aspects | | Very Poor | Satisfactory | Very Good | Marks | | |  |
| 1 | 2 | 3 |
| CLO 1 : Apply the simulation results for the various types of simulation analysis based on the electronic circuit theory and operations.    CLO 2: Construct the simulation and the PCB layout for digital and analogue circuits using a schematic capture software.    CLS 1:  Knowledge &  Understanding    CLS3a :  Practical skill | | | | PART  A    5.1 | **Draw circuit:** Student able to draw the circuit same as given. | | Able to draw the circuit with assistance. | Good to draw the circuit moderately with little assistance. | Excellent to draw  the circuit effectively. | /3 | |  | /3 |
| **Input and analysis setup:** Student able to set the input and transient. | | Able to set the input and transient with assistance. | Good to set the input and transient moderately with little assistance. | Excellent to set the input and transient effectively. | /3 | |  | /3 |
| **Timing**  **Diagram:**  Student able to obtain the output for A, B, S and C correctly. | | Able to obtain the output for A, B, S and C correctly with assistance. | Able to obtain the output for A, B, S  and C correctly  with little assistance. | Able to obtain the output for A, B, S and C effectively. | /3 | |  | /3 |
|  | | | | |  | /9 | |  | /9 |
| PART  A    5.2 | **Draw circuit:** Student able to draw the circuit same as given. | | Able to draw the circuit with assistance. | Good to draw the circuit moderately with little assistance. | Excellent to draw  the circuit effectively. | /3 | |  | /3 |
| **Input and analysis setup:** Student able to set the input and transient. | | Able to set the input and transient with assistance. | Good to set the input and transient moderately with little assistance. | Excellent to set the input and transient effectively. | /3 | |  | /3 |
| **Timing**  **Diagram:**  Student able to obtain the output for A, B, Ci, S and  Co correctly. | | Able to obtain the output for A, B, Ci, S and Co correctly with assistance. | Able to obtain the output for A, B, Ci, S and Co correctly with little assistance. | Able to obtain the  output for A, B, Ci, S and Co  effectively. | /3 | |  | /3 |
|  | | | | |  | /9 | |  | /9 |

# PRACTICAL SKILLS PSYCHOMOTOR ASSESMENT - (80%)

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| **NO.** | **STUDENT’S NAME** | **PART**  **A**    **(5.1)** | **PART**  **A**    **(5.2)** | **Total:** | **80%** |
| **(18 marks)** |
| **A** | **CHONG KHENG CHEN** | /9 | /9 | /18 | /80 |

# PRACTICAL WORK COGNITIVE ASSESSMENT - (REPORT 20%)

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| **PART A TRUTH TABLE** | | **PART B**  **TIMING**  **DIAGRAM** | | **DISCUSSION** | **CONCLUSION** | **TOTAL** | **20%** |
| 5.1 | 5.2 | 5.1 | 5.2 |  |  |  |  |
| /10 | /5 | /5 | /5 | /10 | /10 | /45 | /20 |

# TOTAL MARKS

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **NO.** | **STUDENT’S NAME** | **COGNITIVE**  **ASSESSMENT**  **(20 %)** | **PSYCHOMOTOR**  **ASSESMENT (80 %)** | **Total:** |
| **(100 %)** |
|  | **CHONG KHENG CHEN** | /20 | /80 | /100 |